Remarks

Applicant appreciates the Examiner's acknowledgement regarding the impropriety of the previous § 102 rejection and that the rejection has been withdrawn. As discussed below, the newly presented § 102(b) rejection of claims 1-25 cannot be maintained because the cited portions of the '090 reference do not correspond to numerous aspects of the claimed invention. Moreover, regarding independent claim 13 and various dependent claims, the Examiner fails to even assert correspondence between the limitations of these claims and the '090 reference. As such, the rejection of these claims must also be withdrawn.

The final Office Action dated December 10, 2008, lists the following sole rejection: claims 1-25 stand rejected under 35 U.S.C. § 102(b) over Bhattacharya (U.S. Patent No. 6,378,090). In this discussion set forth below, Applicant does not acquiesce to any rejection or averment in the instant Office Action unless Applicant expressly indicates otherwise.

Applicant respectfully traverses the § 102(b) rejection of claims 1-25 because the cited portions of the '090 reference do not correspond to aspects of the claimed invention directed to a global enable signal that is provided to each of the modules for placing the modules in a test mode. The cited portions of the '090 reference do not teach that the disable TMS signal (*i.e.*, the asserted global enable signal) is provided to each of the embedded cores 720 and 730 (*i.e.*, the asserted modules) for placing the cores 720 and 730 in a test mode. Instead, the cited portions of the '090 reference teach that the disable TMS signal is used to prevent the embedded cores 720 and 730 from receiving the test mode select TMS signal. *See, e.g.*, Figures 7 and 11, and Col. 12:6-13. Thus, the disable TMS signal prevents the embedded cores 720 and 730 from entering the test mode, which is consistent with the '090 reference aptly calling the signal a disable test mode select signal. As such, the disable TMS signal of the '090 reference does not correspond to Applicant's global enable signal. Accordingly, the § 102(b) rejection of claims 1-25 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 102(b) rejection of claims 13-25 because the Examiner fails to assert correspondence between the '090 reference and these claims. Applicant has reviewed the cited portions of the '090 reference and submits that these

portions do not correspond to the claimed invention. For example, the cited portions of the '090 reference do not teach or suggest aspects of the claimed invention directed to a plurality of modules connected in series to a test access mechanism, where, while one of the modules is being tested, the other modules are placed in a transport mode. The cited portions of the '090 reference do not teach that cores 720 and 730 (*i.e.,* the asserted modules) are connected in series or that the other cores 720 or 730 are placed in a transport mode of operation while one of the cores 720 or 730 is being tested. *See, e.g.,* Figure 7. More specifically, the cited portions of the '090 reference teach that the embedded test access ports 727 and 737 (of cores 720 and 730) receive test data input from programmable switch 740 (*i.e.,* the asserted test access mechanism) and that they supply their test data outputs only to programmable switch 740. *See, e.g.,* Col. 8:30-34. Thus, the cores 720 and 730 are individually connected to the programmable switch 740 such that test input data is sent directly from the programmable switch 740 to each of the cores and test output data is sent directly from each of the cores to the programmable switch 740. As such, the cited portions of the '090 reference do not teach placing the other modules in a transport mode, in which test stimulus and test response data is not corrupted by the other modules, in order to enable the other modules to be used to transport the test stimulus data to and test response data from the module being tested. Accordingly, the § 102(b) rejection of claims 13-25 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 102(b) rejection of dependent claims 2-12 and 14-25 because the Examiner fails to assert correspondence between the '090 reference and these claims as required. Applicant notes that the rejection of claims 2-12 and 14-25 presented in the instant Office Action consists solely of discussion of the '090 reference without any explanation regarding how the '090 reference allegedly corresponds to the various limitations found in claims 2-12 and 14-25. In an effort to facilitate prosecution, Applicant has reviewed the cited portions of the '090 reference; however, Applicant submits that the cited portions do not correspond to numerous aspects found in Applicant's dependent claims.

As a first example, regarding claims 5 and 18, the cited portions of the '090 reference do not teach or suggest that each of the control circuits is an OR gate. Instead,

the cited portions of the '090 reference teach using AND gates 741 and 743. *See, e.g.,* Figure 7.

As a second example, regarding claims 10 and 23, the cited portions of the '090 reference do not teach or suggest loading the test stimulus data into the module being tested from another one of the modules in a pipelined manner or unloading the test response data from the module being tested into a further one of the modules in a pipelined manner. As discussed above, the cores 720 and 730 (*i.e.,* the asserted modules) are individually connected to the programmable switch 740 such that test input data is sent directly from the programmable switch 740 to each of the cores and test output data is sent directly from each of the cores to the programmable switch 740. As such, test stimulus data is not loading into the core being tested from the other core and test response data is not unloaded from the core being tested into the other core.

As a third example, regarding claims 2 and 15, the cited portions of the '090 reference do not teach or suggest that each of the control circuits is controlled by a dedicated bypass signal. The cited portions of the '090 reference teach AND gates 741 and 743 (*i.e.,* the asserted control circuits) receive test mode select signals TMS2 and TMS3 and that they also receive disable TMS signal. *See, e.g.,* Figure 7. Applicant submits that the TMS2 and TMS3 signals are not bypass signals because these signals are used to initiate the test mode in core 720 and 730 respectively. Applicant further submits that the disable TMS signal (erroneously asserted by the Examiner as corresponding to Applicant's global enable signal) is not a dedicated bypass signal because the disable TMS signal prevents both of the cores 720 and 730 from entering the test mode as discussed above. As such, the cited portions of the '090 reference do not teach that AND gates 741 and 743 are each controlled by a dedicated bypass signal.

In view of the above, the cited portions of the '090 reference do not correspond to numerous aspects of the claimed invention. Accordingly, the § 102(b) rejection of claims 2-12 and 14-25 is improper and Applicant request that it be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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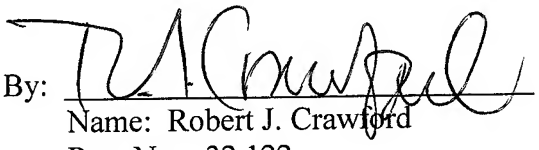
By: 

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